PATENT ABSTRACTS OF JAPAN

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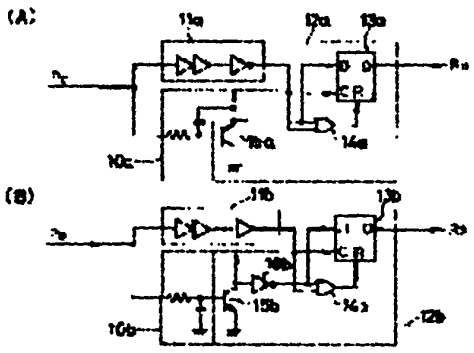
(54) PLL CIRCUIT

(57)Abstract:
PURPOSE: To improve S/N of the PLL circuit in the frequency synthesizer of a reception system by providing a dead zone for phase comparison and realizing stable synchronous convergence.
CONSTITUTION: A phase leading PD pulse is delayed by a delay device 11b and is inputted to the clock input of a D-FF 13b. The PD pulse is integrated by a time constant circuit 10b, and this integral waveform is compared with the threshold of a transistor TR 15b, and, a pulse is generated when it is larger than this threshold. This pulse is inputted to the data input of the D-FF 13b to latch the PD pulse, and the D-FF 13b is reset by an OR gate 14b at the time of disappearance of the PD pulse. Its Q output RD is supplied to a charge pump and a loop filter to obtain the control voltage of a VCO. Consequently, the dead zone is determined by CR of the time constant circuit 10b and the threshold of the TR 15b, and the PD pulse larger than the dead zone is outputted as it is, and therefore, synchronous convergence is stabilized.



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CLAIMS

[Claim(s)]

[Claim 1] An armature-voltage control oscillation means and a phase-comparison means to make the phase comparison of this oscillation output frequency signal and external oscillation signalling frequency, It is a PLL circuit including a control-voltage generation means to generate the control voltage of the aforementioned armature-voltage control oscillation means according to this phase-comparison output. the aforementioned control-voltage generation means A delay means by which the aforementioned phase-comparison output is delayed, and the time constant circuit which considers the aforementioned phase-comparison output as an input, The PLL circuit characterized by being constituted including a latch means to cancel this latch state when the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears by the output of the aforementioned delay means so that the aforementioned control voltage may be generated using this latch output.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] Especially this invention relates to the PLL circuit used in order to obtain the stable synchronizing signal in strange recovery technology about a PLL (phase locked loop) circuit.
[0002]
[Description of the Prior Art] A PLL circuit detects the phase contrast of the reference frequency signal given from the outside, and the dividing output which carried out dividing of the oscillation output of VCO (voltage controlled oscillator), controls VCO by direct current voltage according to the phase contrast, and obtains a stable oscillation output.
[0003] In the receiving system, it mixed with the receiving RF signal by having made this oscillation output into the local oscillation signal, and the IF signal was created and alignment has been obtained for the frequency change at the time of a channel change by changing the division ratio of a counting-down circuit (program divider), or using a direct digital synthesizer etc. and changing the reference frequency signal itself to the source of a signal.
[0004] In local oscillation frequency synthesizer SASHIZA, for a high-speed frequency change, the high interest profit design of a system is performed, but on the other hand noise bandwidth becomes large, it is easy to incorporate noise in a system, and C/N-ary of an oscillation output pose a problem. The method of extending the neutral zone (DETTO zone) in a phase comparison as a negative measure in such a case is taken.
[0005] Drawing 5 is the circuit diagram showing the portion of the phase comparator of the conventional PLL circuit shown in JP,63-260317,A. reference frequency signal fR with which the 1st D-FF and 23 were impressed to the 2nd D-FF, and 24 was impressed [21] to the clocked-into terminal of 1st D-FF22 for a charge pump and 22 The 1st delayed delay circuit and dividing signal fP with which 25 was impressed to the clocked-into terminal of 2nd D-FF23 It is the 2nd delayed delay circuit. 25 and 24 are delay circuits and 28 and 29 are the DETTO zone expansion signal DZ. It is the circuit which responds and chooses the amount of delay.
[0006] Next, operation is explained. input terminal D1 of D-FF22 **** -- reversal output Q2 of D-FF it impresses -- having -- input terminal D2 of D-FF23 **** -- reversal output Q1 of D-FF22 it impresses -- having -- output Q1 it is impressed by the gate of NMOS26 of the charge pump circuit 21 -- having -- output Q2 It is impressed by the gate of NMOS27.
[0007] DETTO zone expansion signal DZ If it turns OFF ("0"), the delay signal of the last stage of a delay circuit will be chosen from selection circuitries 28 and 29.
[0008] First, dividing signal fP It receives and is the reference frequency signal fR. It is fP, as it is shown in drawing 6 (A), when the phase is in agreement. fR By the standup, both D-FF 22 and 23 incorporate a mutual reversal output "1", and it is an output Q1 respectively. And Q2 It outputs. These outputs Q1 and Q2 It goes up by the inclination shown as a solid line like drawing 6 (C), and is threshold voltage Vt. It is TD the time of reaching. Output R1 of selection circuitries 28 and 29 R2 It starts.
[0009] That is, the amount of the maximum delay of delay circuits 24 and 25 is TD. It has designed so that it may become equal, and it is an output R1 and R2. It is reset and both D-FF 22 and 23 are outputs Q1 and Q2. It falls, therefore neither of NMOSes 26 and 27 turn on in this case, and the output PD according to phase contrast is not outputted.
[0010] As shown by drawing 6 (B), after fR ' has become early for 10ns, D-FF22 incorporates "1" and is an output Q1. It starts like dotted-line ** of (C). It is behind for 10ns and D-FF23 is fP. "1" is incorporated in a standup and it is the output Q2. It goes up. Next, when R1 ' is outputted from a selection circuitry 28, it is reset and D-FF23 is an output Q2. Vt Before reaching, it falls like dashed line ** of (C).
[0011] On the other hand, it is the output Q1 of D-FF22. Vt It reaches and is the output R2 of a selection circuitry 29. D-FF22 will be reset. Therefore, output Q1 Vt The period which became above, and NMOS26 are turned on, and the output PD according to phase contrast "0" is outputted. That is, in the case of drawing 6 (C), it is fR. When it becomes early, it is an output R2. Before being outputted, it is surely Vt. Reaching, a dead zone serves as zero.
[0012] Next, DZ= "1" is a case and, as for drawing 6 (D), the delay signal with few amounts of delay than the time of DZ=

"0" is chosen. It is f R first. fP When the phase is in agreement, it is the output R1 of a delay circuit. R2 What is generated is TD. Since it becomes early, it is Q1. Q2 Vt D-FF 22 and 23 is reset without reaching.
[0013] Now and output R1 R2 TD It is fR when it is a delay signal early for 10ns. When it becomes early for 10ns like drawing 6 (D), it is the output Q1 of D-FF22. It goes up, as shown by the solid line of (D), and it is Vt. Since an output R2 occurs just before reaching, D-FF22 is reset, and it is Q1. It falls.
[0014] Therefore, in the case of drawing 6 (E), it is fR. fP Phase contrast is an output Q1 within in 10ns. Vt Output PD corresponding to [before reaching D-FF22 will surely be reset and NMOS26 is turned on, and] phase contrast It is not generated. That is, the dead zone for 10ns is prepared. the same -- fP if it comes out 10 or less ns when it becomes earlier than fR -- output Q2 of D-FF23 Vt Since D-FF23 is reset before reaching, the dead zone for 10ns occurs.
[0015] By preparing a dead zone, frequent generating of a control pulse which serves as disturbance of VCO in the state where the PLL circuit locks was prevented, and noise signals, such as a jitter nozzle, were also omitted, and S/N is improved sharply.
[0016]
[Problem(s) to be Solved by the Invention] In the PLL circuit constituted from a conventional phase-comparison circuit mentioned above, there is a problem on which the reaction of a system becomes slow to the phase contrast near the dead zone.
[0017] For example, fR fP When the case where received and it becomes early for 12ns is assumed, it comes to be shown in drawing 7 . In the state of the dead zone 0 of DZ = "0", it is an output Q1. Vt It can put at about 12ns and the time it is over is PD. Although "1" is outputted for 12ns as a signal a dead-zone 10ns [of DZ = "1"] state -- output Q1 Vt about 2ns of time to exceed -- becoming -- PD As a signal, for 2ns continues but the rate of the integration voltage value change which controls VCO which lets a loop filter pass boils "1" dully.
[0018] If the property of this phase comparison is shown in drawing, it will become like drawing 8 . fR fP Since the time which sees relatively and is deleted in 10ns for the dead-zone setup becomes small when phase contrast is large, although influence decreases, the sensitivity as a remarkable system deteriorates near the dead zone.
[0019] Specifically, although it is convenient to change to near shift frequency at the time of the change of the oscillation frequency of a PLL circuit, alignment near a convergence value is affected and there is a trouble which the phenomenon in which vibration drags on to a convergence value tends to produce.
[0020] The purpose of this invention is offering the PLL circuit which enabled stable synchronous convergence, preparing a dead zone at the time of a phase comparison.
[0021]
[Means for Solving the Problem] A phase-comparison means to make the phase comparison of an armature-voltage control oscillation means, and this oscillation output frequency signal and external oscillation signalling frequency according to this invention, It is a PLL circuit including a control-voltage generation means to generate the control voltage of the aforementioned armature-voltage control oscillation means according to this phase-comparison output. the aforementioned control-voltage generation means A delay means by which the aforementioned phase-comparison output is delayed, and the time constant circuit which considers the aforementioned phase-comparison output as an input, When the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears by the output of the aforementioned delay means, the PLL circuit characterized by being constituted including a latch means to cancel this latch state so that the aforementioned control voltage may be generated using this latch output is obtained.
[0022]
[Example] It explains in detail, referring to a drawing about the example of this invention below.
[0023] Drawing 1 is the block diagram of the example of this invention, and is reference frequency fR. The output of generated VCO 1 turns into one input of a phase comparator 3. Frequency fP which carried out dividing of the oscillation frequency of VCO7 to the other inputs of this phase comparator 3 with the counting-down circuit 2 The signal is impressed.

[0024] It is the lead signal PD of the pulse width according to the phase contrast from a phase comparator 3. It is behind, Signal PU is outputted and it is inputted into filter circuits 4a and 4b, respectively. These filter circuits 4a and 4b are circuits of the feature portion of this invention, and the one example is shown in drawing 2 . They are PD and PU, a dead zone being set up in these filter circuits 4a and 4b. Phase contrast signals RU and RD with which pulse width (phase contrast information is included) does not change It is generated.
[0025] These phase contrast signals RU and RD It becomes the control voltage of VCO7 by being inputted into a loop filter 6 and finding the integral through the charge pump 5.
[0026] The output of this VCO7 serves as local oscillation frequency in a receiving system, change instructions of a receiving channel are answered, the oscillation frequency fR of reference frequency VCO 1 and the division ratio of the program divider 2 are controlled, and the PLL frequency synthesizer is constituted.
[0027] Drawing 2 (A) and (B) are each example circuit diagram of the filter circuits 4a and 4b of drawing 1 . First, if

drawing 2 (A) is referred to, it is the lead signal PU. It is inputted into delay circuit 11a and time constant circuit 10a, respectively. The delay output of delay circuit 11a turns into a clocked into of D-FF13a which constitutes latch circuit 12a.
[0028] The output of time constant circuit 10a turns into a base input of PNP transistor 15a which constitutes latch circuit 12a, and the emitter output of this transistor 15a turns into one input of OR-gate 14a while turning into a data input of D-FF13a. The delay output of delay circuit 11a is impressed to the other inputs of this OR-gate 14a, or the output is the reset input of D-FF13a. And the reversal Q output of D-FF13a is RU. It becomes.
[0029] Drawing 2 (B) is the delay signal PD. Although it consists of delay circuit 11b, time constant circuit 10b, and latch circuit 12b concretely also about the side The polarity of the power supply line of time constant circuit 10b and the polarity of transistor 15b in a latch circuit progress, and it is Signal PU. It has become contrary to a side. Moreover, the collector output of transistor 15b is inverted in inverter 16b, and is the data input of D-FF13b, and one input of OR-gate 14b.
[0030] Drawing 3 is each signal wave form view showing operation of the circuit of drawing 2 (B), and is fR. fP When it receives and a phase is overdue, it is the delay signal PD. Two PDs from which it is a thing at the time of being outputted, and it is behind in this example, and a degree differs The pulse is shown.
[0031] PD shown in (C) A pulse is changed into the loose wave (integration wave) of the standup shown in (d) with the time constant of time constant circuit 10b. This wave is the threshold Vt of transistor 15b. PD which is not attained By the pulse, transistor 15b does not turn on and, therefore, the data input signal (D input signal) from inverter 16b to D-FF13b is not generated. On the other hand, an integration wave is Threshold Vt. PD to attain By the pulse, transistor 15b is generated, as it turns on and a data input signal shows (e) from inverter 16b, and for this data input signal, an integration wave is Threshold Vt. It is generated until it becomes smallness.
[0032] the clocked into of D-FF13b -- PD a pulse -- time tD only -- **** delay PD shown in delayed (f) The pulse is supplied. Here, it is a time delay tD. Same [in the time tM (refer to drawing (e)) to become settled with the time constant of time constant circuit 10b / almost] or it is tM. tD If it selects to smallness a little, it synchronizes with the standup timin timing of a clock signal (delay pulse PD), and a data input signal is incorporated and latched to D-FF13b.
[0033] Delay PD It is the filter circuit output RD which a latch state is reset and is shown in (g) as a result since D-FF13b will be reset by the output of OR-gate 14b, if a pulse falls. It will be obtained.
[0034] Therefore, lead signal PD according to phase contrast Therefore, it is the threshold Vt of filter circuit 12b, without being inputted into the latter charge pump 5 by letting filter circuit 4b (drawing 1) pass depending on the degree of the phase contrast. Time tM to become settled It becomes a dead zone.
[0035] phase-lead-lag-network signal PD exceeding a dead zone ******** -- without the wave of the pulse changing, since there is no bird clapper dully like the former comparatively, the thing of the integration [by which it is outputted to the charge pump 5] voltage value change which controls [near the dead zone / come out and] VCO7 shown in drawing 4 as a phase-comparison property is obtained
[0036] In addition, outputs RU and RD of filter circuits 4a and 4b PU and PD Receiving time delay TD If it attaches, it is a dead zone tM. It can compare and ignore at the convergence time (order for 1 or less ms) demanded also as 100ns (10MHZ) or more than it at the time of the channel change of local oscillation frequency.
[0037] Stopping at the circuit of drawing 2 only being shown in an example, it is clear for various circuit deformation to be possible.
[0038]
[Effect of the Invention] There is an effect that a highly efficient PLL circuit without vibration near the convergence value or a tailing phenomenon is realizable, at the time of a channel change, setting up the dead zone in a phase comparison, when PLL is designed by high interest profit for the high-speed channel change which was described above and which is demanded in a PLL receiving system like according to this invention.
[0039] If it states quantitatively, there is an improvement of 10dB or more with an S/N value, and shortening for 2ms or more can be aimed at in channel change convergence time.

[Translation done.]

TECHNICAL FIELD

[Industrial Application] Especially this invention relates to the PLL circuit used in order to obtain the stable synchronizing signal in strange recovery technology about a PLL (phase locked loop) circuit.

[Translation done.]

PRIOR ART

[Description of the Prior Art] A PLL circuit detects the phase contrast of the reference frequency signal given from the outside, and the dividing output which carried out dividing of the oscillation output of VCO (voltage controlled oscillator), controls VCO by direct current voltage according to the phase contrast, and obtains a stable oscillation output.
[0003] In the receiving system, it mixed with the receiving RF signal by having made this oscillation output into the local oscillation signal, and the IF signal was created and alignment has been obtained for the frequency change at the time of a channel change by changing the division ratio of a counting-down circuit (program divider), or using a direct digital synthesizer etc. and changing the reference frequency signal itself to the source of a signal.
[0004] In local oscillation frequency synthesizer SASHIZA, for a high-speed frequency change, the high interest profit design of a system is performed, but on the other hand noise bandwidth becomes large, it is easy to incorporate noise in a system, and C/N-ary of an oscillation output pose a problem. The method of extending the neutral zone (DETTO zone) in a phase comparison as a negative measure in such a case is taken.
[0005] For a charge pump and 22, 21 is the reference frequency signal fR with which drawing 5 was the circuit diagram showing the portion of the phase comparator of the conventional PLL circuit shown in JP,63-260317,A, the 1st D-FF and 23 were impressed to the 2nd D-FF, and 24 was impressed to the clocked-into terminal of 1st D-FF22. 25 is the 1st delayed delay circuit and the dividing signal fP impressed to the clocked-into terminal of 2nd D-FF23. It is the 2nd delayed delay circuit. 25 and 24 are delay circuits and 28 and 29 are the DETTO zone expansion signal DZ. It is the circuit which responds and chooses the amount of delay.
[0006] Next, operation is explained. input terminal D1 of D-FF22 **** -- reversal output Q2 of D-FF it impresses -- having -- input terminal D2 of D-FF23 **** -- reversal output Q1 of D-FF22 it impresses -- having -- output Q1 it is impressed by the gate of NMOS26 of the charge pump circuit 21 -- having -- output Q2 It is impressed by the gate of NMOS27.
[0007] DETTO zone expansion signal DZ If it turns OFF ("0"), the delay signal of the last stage of a delay circuit will be chosen from selection circuitries 28 and 29.
[0008] First, dividing signal fP It receives and is the reference frequency signal fR. It is fP, as it is shown in drawing 6 (A), when the phase is in agreement. fR By the standup, both D-FF 22 and 23 incorporate a mutual reversal output "1", and it is an output Q1 respectively. And Q2 It outputs. These outputs Q1 and Q2 It goes up by the inclination shown as a solid line like drawing 6 (C), and is threshold voltage Vt. It is TD the time of reaching. Output R1 of selection circuitries 28 and 29 R2 It starts.
[0009] That is, the amount of the maximum delay of delay circuits 24 and 25 is TD. It has designed so that it may become equal, and it is an output R1 and R2. It is reset and both D-FF 22 and 23 are outputs Q1 and Q2. It falls, therefore neither of NMOSes 26 and 27 turn on in this case, and the output PD according to phase contrast is not outputted.
[0010] As shown by drawing 6 (B), after fR ' has become early for 10ns, D-FF22 incorporates "1" and is an output Q1. It starts like dotted-line ** of (C). It is behind for 10ns and D-FF23 is fP. "1" is incorporated in a standup and it is the output Q2. It goes up. Next, when R1 ' is outputted from a selection circuitry 28, it is reset and D-FF23 is an output Q2. Vt Before reaching, it falls like dashed line ** of (C).
[0011] On the other hand, it is the output Q1 of D-FF22. Vt It reaches and is the output R2 of a selection circuitry 29. D-FF22 will be reset. Therefore, output Q1 Vt The period which became above, and NMOS26 are turned on, and the output PD according to phase contrast "0" is outputted. That is, in the case of drawing 6 (C), it is fR. When it becomes early, it is an output R2. Before being outputted, it is surely Vt. Reaching, a dead zone serves as zero.
[0012] Next, DZ= "1" is a case and, as for drawing 6 (D), the delay signal with few amounts of delay than the time of DZ= "0" is chosen. It is f R first. fP When the phase is in agreement, it is the output R1 of a delay circuit. R2 What is generated is TD. Since it becomes early, it is Q1. Q2 Vt D-FF 22 and 23 is reset without reaching.
[0013] Now and output R1 R2 TD It is fR when it is a delay signal early for 10ns. When it becomes early for 10ns like drawing 6 (D), it is the output Q1 of D-FF22. It goes up, as shown by the solid line of (D), and it is Vt. Since an output R2 occurs just before reaching, D-FF22 is reset, and it is Q1. It falls.

[0014] Therefore, in the case of drawing 6 (E), it is fR. fP Phase contrast is an output Q1 within in 10ns. Vt Output PD corresponding to [before reaching D-FF22 will surely be reset and NMOS26 is turned on, and] phase contrast It is not generated. That is, the dead zone for 10ns is prepared. the same -- fP if it comes out 10 or less ns when it becomes earlier than fR -- output Q2 of D-FF23 Vt Since D-FF23 is reset before reaching, the dead zone for 10ns occurs.
[0015] By preparing a dead zone, frequent generating of a control pulse which serves as disturbance of VCO in the state where the PLL circuit locks was prevented, and noise signals, such as a jitter nozzle, were also omitted, and S/N is improved sharply.

[Translation done.]

EFFECT OF THE INVENTION

[Effect of the Invention] There is an effect that a highly efficient PLL circuit without vibration near the convergence value or a tailing phenomenon is realizable, at the time of a channel change, setting up the dead zone in a phase comparison, when PLL is designed by high interest profit for the high-speed channel change which was described above and which is demanded in a PLL receiving system like according to this invention.
[0039] If it states quantitatively, there is an improvement of 10dB or more with an S/N value, and shortening for 2ms or more can be aimed at in channel change convergence time.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] In the PLL circuit constituted from a conventional phase-comparison circuit mentioned above, there is a problem on which the reaction of a system becomes slow to the phase contrast near the dead zone.

[0017] For example, fR fP When the case where received and it becomes early for 12ns is assumed, it comes to be shown in drawing 7 . In the state of the dead zone 0 of DZ = "0", it is an output Q1. Vt It can put at about 12ns and the time it is over is PD. Although "1" is outputted for 12ns as a signal a dead-zone 10ns [of DZ = "1"] state -- output Q1 Vt about 2ns of time to exceed -- becoming -- PD As a signal, for 2ns continues but the rate of the integration voltage value change which controls VCO which lets a loop filter pass boils "1" dully.

[0018] If the property of this phase comparison is shown in drawing, it will become like drawing 8 . fR fP Since the time which sees relatively and is deleted in 10ns for the dead-zone setup becomes small when phase contrast is large, although influence decreases, the sensitivity as a remarkable system deteriorates near the dead zone.

[0019] Specifically, although it is convenient to change to near shift frequency at the time of the change of the oscillation frequency of a PLL circuit, alignment near a convergence value is affected and there is a trouble which the phenomenon in which vibration drags on to a convergence value tends to produce.

[0020] The purpose of this invention is offering the PLL circuit which enabled stable synchronous convergence, preparing a dead zone at the time of a phase comparison.

[Translation done.]

MEANS

[Means for Solving the Problem] They are the time constant circuit which is the PLL circuit which includes an armature-voltage-control oscillation means, a phase-comparison means make the phase comparison of this oscillation output-frequency signal and external oscillation signalling frequency, and a control-voltage generation means generate the control voltage of the aforementioned armature-voltage-control oscillation means according to this phase-comparison output according to this invention, and the aforementioned control-voltage generation means carries out as an input in a delay means to by_which the aforementioned phase-comparison output is delayed, and the aforementioned phase-comparison output, and the output of the aforementioned delay means. When the output state of the aforementioned time constant circuit is latched and the output of the aforementioned delay means disappears, the PLL circuit characterized by being constituted including a latch means to cancel this latch state so that the aforementioned control voltage may be generated using this latch output is obtained.

[Translation done.]

EXAMPLE

[Example] It explains in detail, referring to a drawing about the example of this invention below.
[0023] Drawing 1 is the block diagram of the example of this invention, and is reference frequency fR. The output of generated VCO 1 turns into one input of a phase comparator 3. Frequency fP which carried out dividing of the oscillation frequency of VCO7 to the other inputs of this phase comparator 3 with the counting-down circuit 2 The signal is impressed.

[0024] It is the lead signal PD of the pulse width according to the phase contrast from a phase comparator 3. It is behind, Signal PU is outputted and it is inputted into filter circuits 4a and 4b, respectively. These filter circuits 4a and 4b are circuits of the feature portion of this invention, and the one example is shown in drawing 2 . They are PD and PU, a dead zone being set up in these filter circuits 4a and 4b. Phase contrast signals RU and RD with which pulse width (phase contrast information is included) does not change It is generated.
[0025] These phase contrast signals RU and RD It becomes the control voltage of VCO7 by being inputted into a loop filter 6 and finding the integral through the charge pump 5.
[0026] The output of this VCO7 serves as local oscillation frequency in a receiving system, change instructions of a receiving channel are answered, the oscillation frequency fR of reference frequency VCO 1 and the division ratio of the program divider 2 are controlled, and the PLL frequency synthesizer is constituted.
[0027] Drawing 2 (A) and (B) are each example circuit diagram of the filter circuits 4a and 4b of drawing 1 . First, if drawing 2 (A) is referred to, it is the lead signal PU. It is inputted into delay circuit 11a and time constant circuit 10a, respectively. The delay output of delay circuit 11a turns into a clocked into of D-FF13a which constitutes latch circuit 12a.
[0028] The output of time constant circuit 10a turns into a base input of PNP transistor 15a which constitutes latch circuit 12a, and the emitter output of this transistor 15a turns into one input of OR-gate 14a while turning into a data input of D-FF13a. The delay output of delay circuit 11a is impressed to the other inputs of this OR-gate 14a, or the output is the reset input of D-FF13a. And the reversal Q output of D-FF13a is RU. It becomes.
[0029] Drawing 2 (B) is the delay signal PD. Although it consists of delay circuit 11b, time constant circuit 10b, and latch circuit 12b concretely also about the side The polarity of the power supply line of time constant circuit 10b and the polarity of transistor 15b in a latch circuit progress, and it is Signal PU. It has become contrary to a side. Moreover, the collector output of transistor 15b is inverted in inverter 16b, and is the data input of D-FF13b, and one input of OR-gate 14b.
[0030] Drawing 3 is each signal wave form view showing operation of the circuit of drawing 2 (B), and is fR. fP When it receives and a phase is overdue, it is the delay signal PD. Two PDs from which it is a thing at the time of being outputted, and it is behind in this example, and a degree differs The pulse is shown.
[0031] PD shown in (C) A pulse is changed into the loose wave (integration wave) of the standup shown in (d) with the time constant of time constant circuit 10b. This wave is the threshold Vt of transistor 15b. PD which is not attained By the pulse, transistor 15b does not turn on and, therefore, the data input signal (D input signal) from inverter 16b to D-FF13b is not generated. On the other hand, an integration wave is Threshold Vt. PD to attain By the pulse, transistor 15b is generated, as it turns on and a data input signal shows (e) from inverter 16b, and for this data input signal, an integration wave is Threshold Vt. It is generated until it becomes smallness.
[0032] the clocked into of D-FF13b -- PD a pulse -- time tD only -- **** delay PD shown in delayed (f) The pulse is supplied. Here, it is a time delay tD. Same [in the time tM (refer to drawing (e)) to become settled with the time constant of time constant circuit 10b / almost] or it is tM. tD If it selects to smallness a little, it synchronizes with the standup timin timing of a clock signal (delay pulse PD), and a data input signal is incorporated and latched to D-FF13b.
[0033] Delay PD It is the filter circuit output RD which a latch state is reset and is shown in (g) as a result since D-FF13b will be reset by the output of OR-gate 14b, if a pulse falls. It will be obtained.
[0034] Therefore, lead signal PD according to phase contrast Therefore, it is the threshold Vt of filter circuit 12b, without being inputted into the latter charge pump 5 by letting filter circuit 4b (drawing 1) pass depending on the degree of the phase contrast. Time tM to become settled It becomes a dead zone.

[0035] phase-lead-lag-network signal PD exceeding a dead zone ******** -- without the wave of the pulse changing, since there is no bird clapper dully like the former comparatively, the thing of the integration [by which it is outputted to the charge pump 5] voltage value change which controls [near the dead zone / come out and] VCO7 shown in drawing 4 as a phase-comparison property is obtained

[0036] In addition, outputs RU and RD of filter circuits 4a and 4b PU and PD Receiving time delay TD If it attaches, it is a dead zone tM. It can compare and ignore at the convergence time (order for 1 or less ms) demanded also as 100ns (10MHZ) or more than it at the time of the channel change of local oscillation frequency.

[0037] Stopping at the circuit of drawing 2 only being shown in an example, it is clear for various circuit deformation to be possible.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the PLL circuit by this invention.
[Drawing 2] It is the circuit diagram showing an example of the filter circuits 4a and 4b of drawing 1 .
[Drawing 3] It is each part operation wave form chart of the circuit of drawing 2 .
[Drawing 4] It is the phase-comparison property view of the PLL circuit by this invention.
[Drawing 5] It is the circuit diagram of the phase comparator of the conventional PLL circuit.
[Drawing 6] It is each wave form chart of the circuit of drawing 5 of operation.
[Drawing 7] It is each wave form chart of the circuit of drawing 5 of operation.
[Drawing 8] It is the phase-comparison property view of the circuit of drawing 5 .
[Description of Notations]
1 Reference Frequency VCO
2 Counting-down Circuit
3 Phase Comparator
4a, 4b Filter circuit
5 Charge Pump
6 Loop Filter
7 VCO
10a, 10b Time constant circuit
11a, 11b Delay circuit
12a, 12b Latch circuit
13a,13b D-FF
14a, 14b OR gate
15a, 15b Transistor
16b Inverter

[Translation done.]

* NOTICES *

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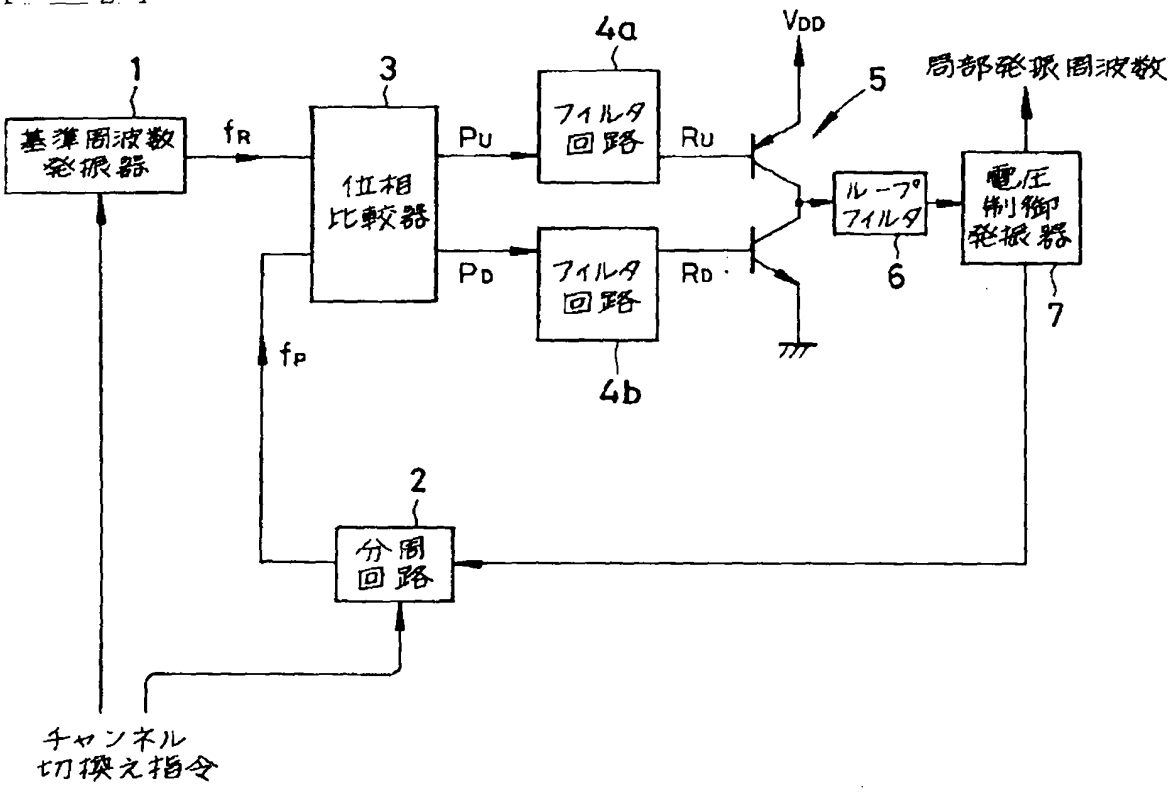
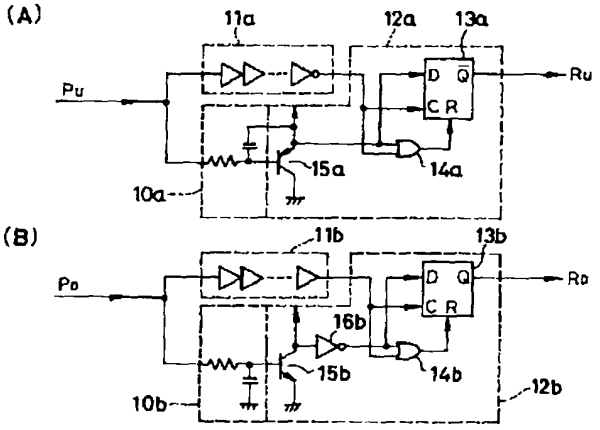
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

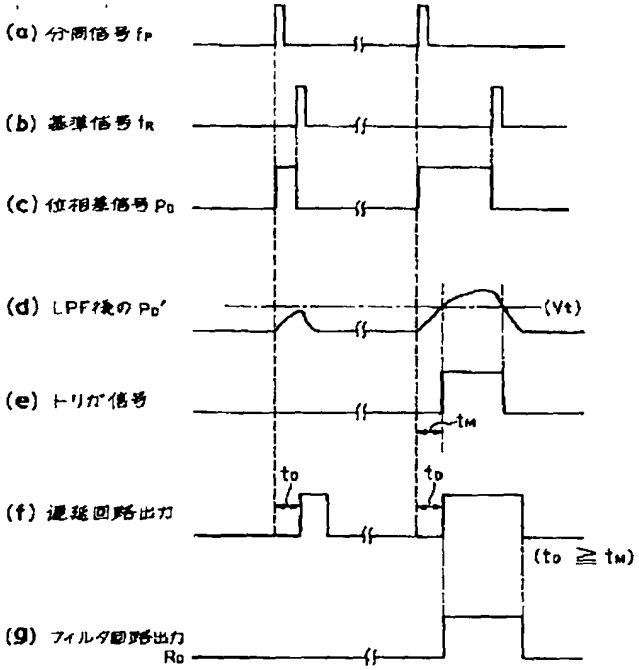
[Drawing 1]



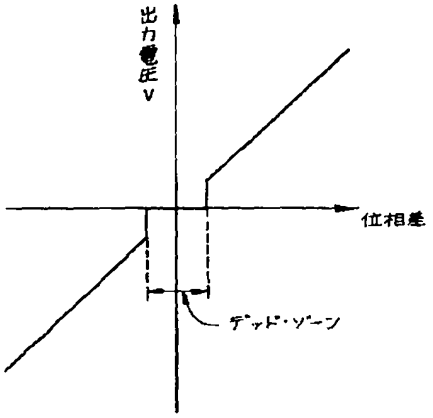
[Drawing 2]



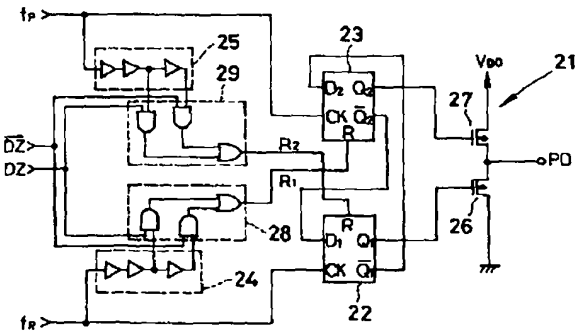
[Drawing 3]



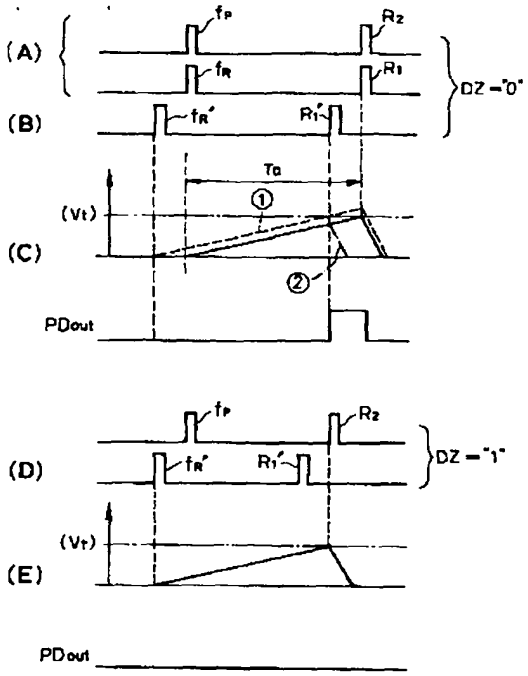
[Drawing 4]



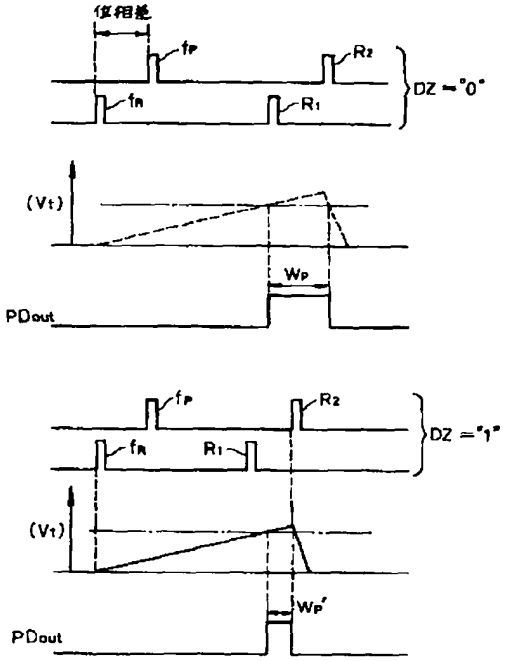
[Drawing 5]



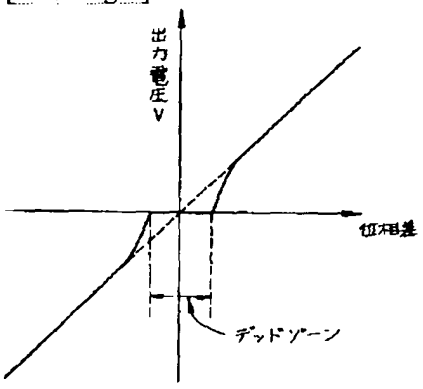
[Drawing 6]



[Drawing 7]



[Drawing 8]



[Translation done.]

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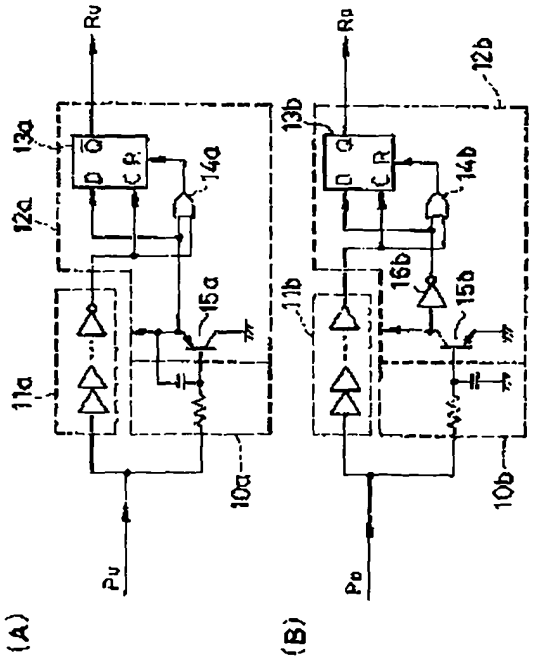
(54)【発明の名称】　ＰＬＬ回路

(57)【要約】

【目的】　受信システムの周波数シンセサイザにおけるＰＬＬ回路のＳ／Ｎ改善のために位相比較にデッドゾーンを設けつつ安定な同期収束を可能とする。

【構成】　位相進みＰｄパルスを遅延器１１ｂで遅延してＤ－ＦＦ１３ｂのクロック入力とする。また、Ｐｄパルスを時定数回路１０ｂで積分し、この積分波形をトランジスタ１５ｂの閾値と比較してこの閾値以上のときにパルスを生成する。このパルスをＤ－ＦＦ１３ｂのデータ入力としてＰｄパルスをラッチし、オアゲート１４ｂでＰｄパルス消滅時にＤ－ＦＦ１３ｂをリセットする。このＱ出力Ｒｄをチャージポンプ，ループフィルタへ供給してＶＣＯの制御電圧を得る。

【効果】　デッドゾーンは時定数回路のＣＲとトランジスタの閾値で定まり、デッドゾーンより大なるＰｄパルスはそのまま出力されるので、同期収束が安定となる。



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【特許請求の範囲】

【請求項1】　電圧制御発振手段と、この発振出力周波数信号と外部発振周波数信号との位相比較をなす位相比較手段と、この位相比較出力に応じて前記電圧制御発振手段の制御電圧を生成する制御電圧生成手段とを含むＰＬＬ回路であって、前記制御電圧生成手段は、前記位相比較出力を遅延する遅延手段と、前記位相比較出力を入力とする時定数回路と、前記遅延手段の出力によって前記時定数回路の出力状態をラッチし前記遅延手段の出力が消失したときにこのラッチ状態を解除するラッチ手段とを含み、このラッチ出力を用いて前記制御電圧を生成するよう構成されていることを特徴とするＰＬＬ回路。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はＰＬＬ（フェイズロックドループ）回路に関し、特に変復調技術における安定な同期信号を得るために用いられるＰＬＬ回路に関する。

【０００２】

【従来の技術】ＰＬＬ回路は、外部から与えられる基準周波数信号と、ＶＣＯ（電圧制御発振器）の発振出力を分周した分周出力との位相差を検出し、その位相差に応じた直流電圧によりＶＣＯを制御して安定な発振出力を得るものである。

【０００３】受信システムにおいて、この発振出力をローカル発振信号として受信ＲＦ信号と混合し、ＩＦ信号を作成するようになっており、チャンネル切換え時の周波数切換えには、分周器（プログラムデバイダ）の分周比を変更するか、あるいは基準周波数信号自体を信号源にダイレクトディジタルシンセサイザ等を用いて変化させることにより同調を得ている。

【０００４】局部発振周波数シンセサンザにおいては、高速の周波数切換えのためには、系の高利得設計が行われるが、その反面雑音帯域幅が大きくなり、系内に雑音を取り込み易く、発振出力のＣ／Ｎ値が問題となる。こうした場合にネガティブな措置として、位相比較における不感帯（デットゾーン）を拡げる方法がとられる。

【０００５】図5は特開昭63－260317号公報に示された従来のＰＬＬ回路の位相比較器の部分を示す回路図であり、２１はチャージポンプ、２２は第１のＤ－ＦＦ、２３は第２のＤ－ＦＦ、２４は第１のＤ－ＦＦ２２のクロック入力端子に印加された基準周波数信号ｆＲを遅延する第１の遅延回路、２５は第２のＤ－ＦＦ２３のクロック入力端子に印加された分周信号ｆＰを遅延する第２の遅延回路である。２５，２４は遅延回路であり、２８，２９はデットゾーン拡大信号ＤＺに応じて遅延量を選択する回路である。

【０００６】次に動作について説明する。Ｄ－ＦＦ２２の入力端子Ｄ1には、Ｄ－ＦＦの反転出力Ｑ2が印加され、Ｄ－ＦＦ２３の入力端子Ｄ2にはＤ－ＦＦ２２の反転出力Ｑ1が印加され、出力Ｑ1はチャージポンプ回路

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２１のＮＭＯＳ２６のゲートに印加され、出力Ｑ2はＮＭＯＳ２７のゲートに印加される。

【０００７】デットゾーン拡大信号ＤＺをオフ（"０"）にすると、遅延回路の最終段の遅延信号が選択回路２８，２９より選択される。

【０００８】まず、分周信号ｆＰに対して基準周波数信号ｆＲの位相が一致しているとき、図６（Ａ）に示す様にｆＰとｆＲの立上りにより、Ｄ－ＦＦ２２，２３は共に互いの反転出力"１"を取込んで各々出力Ｑ1及びＱ2に出力する。この出力Ｑ1及びＱ2は、図６（Ｃ）の様に実線で示される傾斜で上昇し、スレッショルド電圧Ｖｔに達する時点ＴＤで選択回路２８，２９の出力Ｒ１とＲ2が立上る。

【０００９】すなわち、遅延回路２４，２５の最大遅延量はＴＤと等しくなる様に設計してあり、出力Ｒ１，Ｒ2によりＤ－ＦＦ２２，２３は共にリセットされ、出力Ｑ1及びＱ2は低下し、従ってこの場合、ＮＭＯＳ２６，２７は共にオンせず、位相差に応じた出力ＰＤは出力されない。

【００１０】図６（Ｂ）で示される如く、ｆＲ′が１０ｎｓｅｃ早くなった状態では、Ｄ－ＦＦ２２は"１"を取込み、出力Ｑ1は（Ｃ）の点線①の様に立上る。Ｄ－ＦＦ２３は１０ｎｓｅｃ遅れてｆＰの立上りで"１"を取込み、その出力Ｑ2が上昇する。次に選択回路２８からＲ１′が出力されると、Ｄ－ＦＦ２３はリセットされ、出力Ｑ2はＶｔに達する前に、（Ｃ）の破線②の様に立下がる。

【００１１】一方、Ｄ－ＦＦ２２の出力Ｑ1はＶｔに達し、選択回路２９の出力Ｒ2によりＤ－ＦＦ２２がリセットされることになる。従って、出力Ｑ1がＶｔ以上になった期間、ＮＭＯＳ２６がオンとなって、位相差に応じた出力ＰＤ"０"が出力される。すなわち、図６（Ｃ）の場合には、ｆＲが早くなると、出力Ｒ2が出力される前に必ずＶｔに達することになり、デッドゾーンは零となるのである。

【００１２】次に図６（Ｄ）はＤＺ＝"１"の場合であり、ＤＺ＝"０"の時より、遅延量の少い遅延信号が選択される。まずｆＲとｆＰの位相が一致している時には、遅延回路の出力Ｒ１とＲ2が発生するのがＴＤより早くなるので、Ｑ1とＱ2はＶｔに達せずにＤ－ＦＦ２２，２３がリセットされる。

【００１３】いま、出力Ｒ１とＲ2がＴＤより１０ｎｓｅｃ早い遅延信号であるとした時、ｆＲが図６（Ｄ）の如く、１０ｎｓｅｃ早くなった場合、Ｄ－ＦＦ２２の出力Ｑ1は（Ｄ）の実線で示される如く上昇し、Ｖｔに達する直前において、出力Ｒ2が発生するためにＤ－ＦＦ２２がリセットされ、Ｑ1は低下する。

【００１４】したがって、図６（Ｅ）の場合には、ｆＲとｆＰの位相差が１０ｎｓｅｃ以内では、出力Ｑ1がＶｔに達する前に必ずＤ－ＦＦ２２がリセットされること

になり、NMOS26がオンとなって位相差に対応する出力PDが発生されることはない。すなわち、10nsecのデッドゾーンが設けられる。同様にfPがfRより早くなった場合は、10nsec以下であれば、D－FF23の出力Q2がVtに達する前にD－FF23がリセットされるので、10nsecのデッドゾーンが発生する。

【0015】デッドゾーンを設けることにより、PLL回路がロックしている状態でVCOの外乱となるような制御パルスの頻繁な発生が防止され、またジッタノズル等の雑音信号もカットされ、S／Nを大幅に改善している。

【0016】

【発明が解決しようとする課題】上述した従来の位相比較回路で構成したPLL回路においては、デッドゾーン近傍での位相差に対して、系の反応が鈍化する問題がある。

【0017】例えば、fRがfPに対して12nsec早くなった場合を想定すると、図7に示す様になる。Dz＝"0"のデッドゾーン0の状態では、出力Q1がVtを越えている時間は約12nsecとみることができ、PD信号として"1"が12nsec出力されるが、Dz＝"1"のデッドゾーン10nsecの状態では、出力Q1がVtを越える時間約2nsecとなり、PD信号として「1」は2nsec間しか続かず、ループフィルタを通してのVCOの制御を行う積分電圧値の変化の割合が鈍くにる。

【0018】この位相比較の特性を図に示すと図8のようになる。fRとfPの位相差が大きい時には、相対的にみてそのデッドゾーン設定分の10nsecで削られる時間が小さくなるため、影響は少くなるが、デッドゾーン近傍でかなり系としての感度は劣化する。

【0019】具体的には、PLL回路の発振周波数の切換時、シフト周波数付近への変化に支障はないが、収束値付近での同調に影響が出て、収束値に対して振動が尾を引く現象が生じ易い問題点がある。

【0020】本発明の目的は、位相比較時にデッドゾーンを設けつつ安定な同期収束を可能としたPLL回路を提供することである。

【0021】

【課題を解決しようとする手段】本発明によれば、電圧制御発振手段と、この発振出力周波数信号と外部発振周波数信号との位相比較をなす位相比較手段と、この位相比較出力に応じて前記電圧制御発振手段の制御電圧を生成する制御電圧生成手段とを含むPLL回路であって、前記制御電圧生成手段は、前記位相比較出力を遅延する遅延手段と、前記位相比較出力を入力とする時定数回路と、前記遅延手段の出力によって前記時定数回路の出力状態をラッチし前記遅延手段の出力が消失したときにこのラッチ状態を解除するラッチ手段とを含み、このラッチ出力を用いて前記制御電圧を生成するよう構成されていることを特徴とするPLL回路が得られる。

【0022】

【実施例】以下に本発明の実施例について図面を参照しつつ詳細に説明する。

【0023】図1は本発明の実施例のブロック図であり、基準周波数fRを発生する発振器1の出力は位相比較器3の一入力となる。この位相比較器3の他入力には、VCO7の発振周波数を分周器2にて分周した周波数fPの信号が印加されている。

【0024】位相比較器3からは、位相差に応じたパルス幅の進み信号PDと遅れ信号PUとが出力され、フィルタ回路4a，4bへ夫々入力される。このフィルタ回路4a，4bが本発明の特徴部分の回路であって図2にその一具体例が示されている。このフィルタ回路4a，4bにおいて、デッドゾーンが設定されつつPD，PUのパルス幅（位相差情報を含んでいる）が変化することのない、位相差信号RU，RDが生成される。

【0025】この位相差信号RU，RDはチャージポンプ5を介してループフィルタ6へ入力され積分されることによりVCO7の制御電圧となる。

【0026】このVCO7の出力が受信システムにおけるローカル発振周波数となっており、受信チャンネルの切換え指令に応答して基準周波数発振器1の発振周波数fR及びプログラムデバイダ2の分周比がコントロールされ、PLL周波数シンセサイザを構成している。

【0027】図2（A），（B）は図1のフィルタ回路4a，4bの各具体例回路図である。まず、図2（A）を参照すると、進み信号PUは遅延回路11a及び時定数回路10aへ夫々入力される。遅延回路11aの遅延出力は、ラッチ回路12aを構成するD－FF13aのクロック入力となる。

【0028】時定数回路10aの出力は、ラッチ回路12aを構成するPNPトランジスタ15aのベース入力となり、このトランジスタ15aのエミッタ出力はD－FF13aのデータ入力となると共に、オアゲート14aの一入力となる。このオアゲート14aの他入力には遅延回路11aの遅延出力が印加され、オア出力はD－FF13aのリセット入力となっている。そして、D－FF13aの反転Q出力がRUとなる。

【0029】図2（B）は遅れ信号PD側についても、具体的に遅延回路11b，時定数回路10b及びラッチ回路12bからなっているが、時定数回路10bの電源ラインの極性、ラッチ回路内のトランジスタ15bの極性が進み信号PU側とは逆となっており、また、トランジスタ15bのコレクタ出力はインバータ16bにて極性反転されてD－FF13bのデータ入力及びオアゲート14bの一入力となっている。

【0030】図3は図2（B）の回路の動作を示す各信号波形図であり、fRがfPに対して位相が遅れたと

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き．遅れ信号PDが出力された場合のものであって、本例では遅れ度合が異なる2つのPDパルスを示している。

【0031】（C）に示すPDパルスは時定数回路10bの時定数によって（d）に示す立上りの緩やかな波形（積分波形）に変換される。この波形がトランジスタ15bの閾値Vtに達しないPDパルスでは、トランジスタ15bはオンせず、よってインバータ16bからD－FF13bへのデータ入力信号（D入力信号）は生成されない。一方．積分波形が閾値Vtに達するPDパルスでは．トランジスタ15bはオンしてインバータ16bからデータ入力信号が（e）に示す如く生成され．このデータ入力信号は積分波形が閾値Vtより小となるまで生成される。

【0032】D－FF13bのクロック入力にはPDパルスが時間tDだけ遅延された（f）に示す如き遅延PDパルスが供給されている。ここで．遅延時間tDと時定数回路10bの時定数により定まる時間tM（図（e）参照）とを略ど同一か若しくはtMをtDより若干小に選定しておけば、クロック信号（遅延パルスPD）の立上りタイミングに同期しD－FF13bにはデータ入力信号が取込まれてラッチされる。

【0033】遅延PDパルスが立下がると、オアゲート14bの出力によりD－FF13bはリセットされるので．ラッチ状態がリセットされ、結果として（g）に示すフィルタ回路出力RDが得られることになる。

【0034】従って、位相差に応じた進み信号PDは、その位相差の度合によってはフィルタ回路4b（図1）を通すことにより後段のチャージポンプ5へ入力されることなく、よってフィルタ回路12bの閾値Vtにより定まる時間tMがデッドゾーンとなるのである。

【0035】デッドゾーンを越える位相進み信号PDについては、そのパルスの波形が変化することなくチャージポンプ5へ出力されるで．デッドゾーン近傍において．VCO7の制御を行う積分電圧値の変化の割合が、従来の如く鈍くなることがないので．位相比較特性としては図4に示すものが得られる。

【0036】尚．フィルタ回路4a．4bの出力RU，RDのPU，PDに対する遅延時間TDについては、デッドゾーンtMを100ns（10MHz）またはそれ以上としても．ローカル発振周波数のチャンネル切換え

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時に要求される収束時間（1ms以下のオーダ）に比し無視できる。

【0037】図2の回路は単に一例に示すに止まるもので．種々の回路変形が可能であることは明らかである。

【0038】

【発明の効果】以上のべた様に、本発明によれば．PLL受信システムにおいて要求される高速チャンネル切換えのために高利得でPLLを設計した場合にも．位相比較におけるデッドゾーンを設定しつつチャンネル切換え時に収束値近傍での振動や尾引き現象を伴うことのない高性能PLL回路が実現できるという効果がある。

【0039】定量的に述べると、S／N値で10dB以上の改善があり．チャンネル切換え収束時間で2ms以上の短縮が図れるものである。

【図面の簡単な説明】

【図1】本発明によるPLL回路のブロック図である。

【図2】図1のフィルタ回路4a，4bの一例を示す回路図である。

【図3】図2の回路の各部動作波形図である。

【図4】本発明によるPLL回路の位相比較特性図である。

【図5】従来のPLL回路の位相比較器の回路図である。

【図6】図5の回路の各動作波形図である。

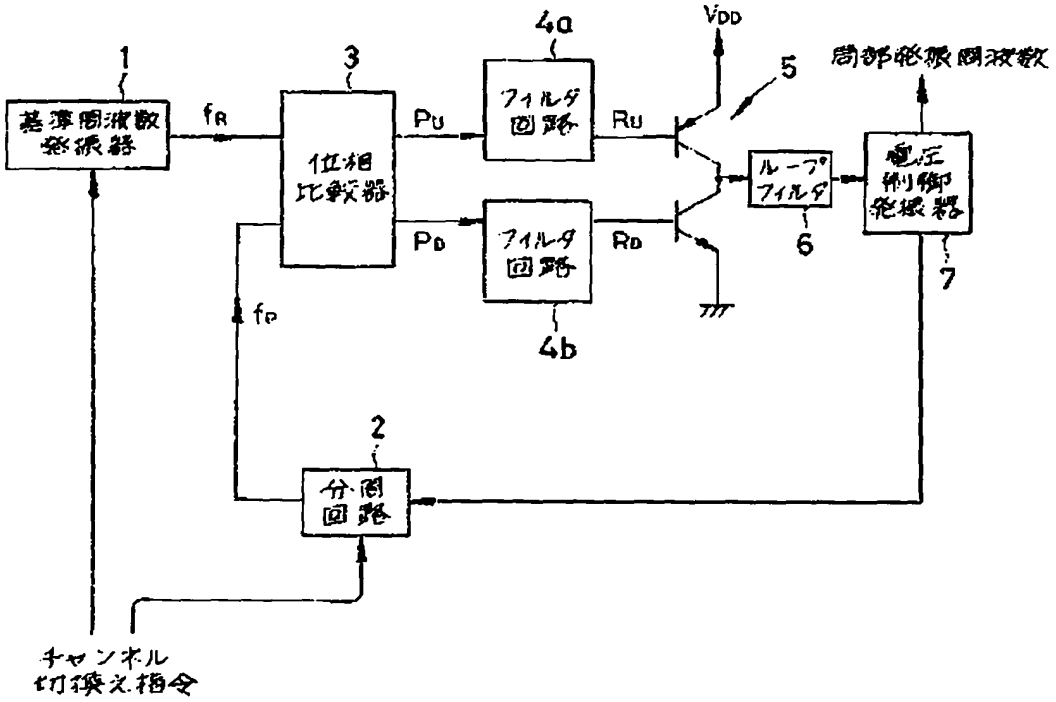
【図7】図5の回路の各動作波形図である。

【図8】図5の回路の位相比較特性図である。

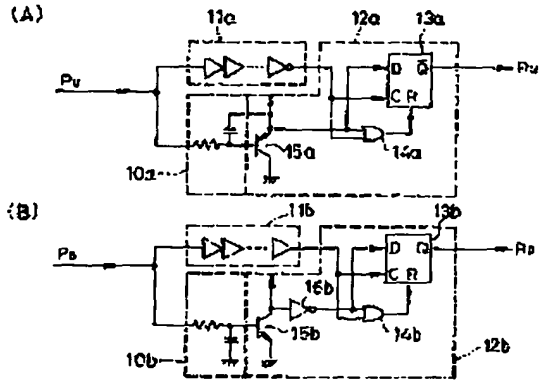
【符号の説明】

1　基準周波数発振器
2　分周器
3　位相比較器
4a，4b　フィルタ回路
5　チャージポンプ
6　ループフィルタ
7　VCO
10a，10b　時定数回路
11a，11b　遅延回路
12a，12b　ラッチ回路
13a，13b　D－FF
14a，14b　オアゲート
15a，15b　トランジスタ
16b　インバータ

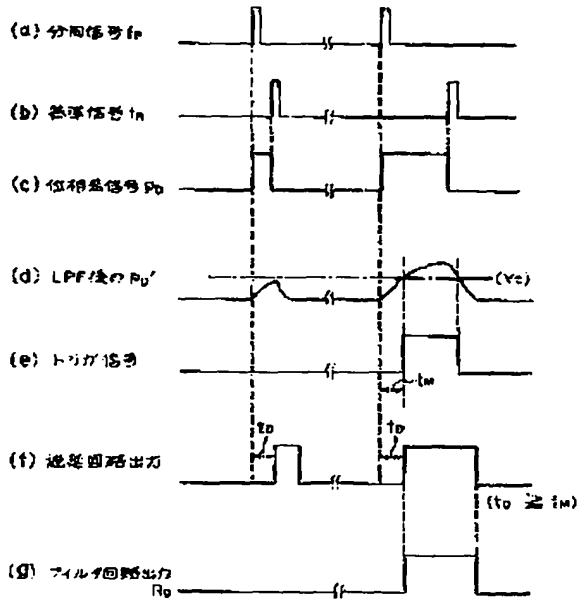
【図1】


基準周波数発振器
位相比較器
フィルタ回路
フィルタ回路
ループフィルタ
電圧制御発振器
分周回路
局部発振周波数
チャンネル切換え指令
VDD
fR
fP
Pu
Pd
Ru
Rd

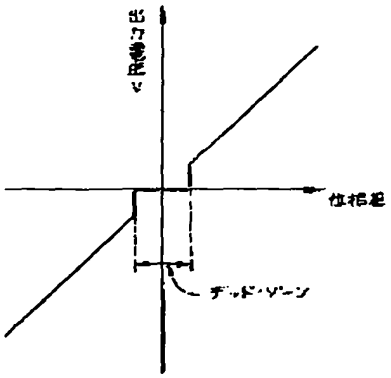
【図2】


(A)
(B)
Pu
Pd
Ru
Rd
15a
14a
15b
14b
16b

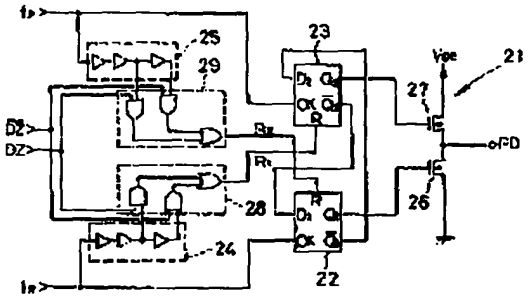
【図3】


(a) 分周信号 fp
(b) 基準信号 fR
(c) 位相差信号 Pd
(d) LPF後の Pd'
(e) トリガ信号
(f) 遅延回路出力
(g) フィルタ回路出力 Rd

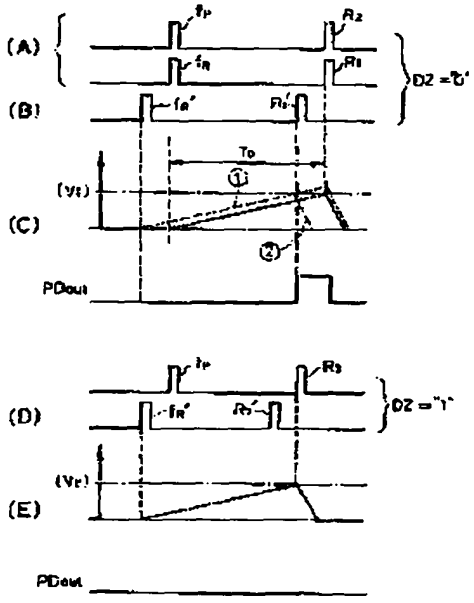
【図4】


位相差
デッドゾーン

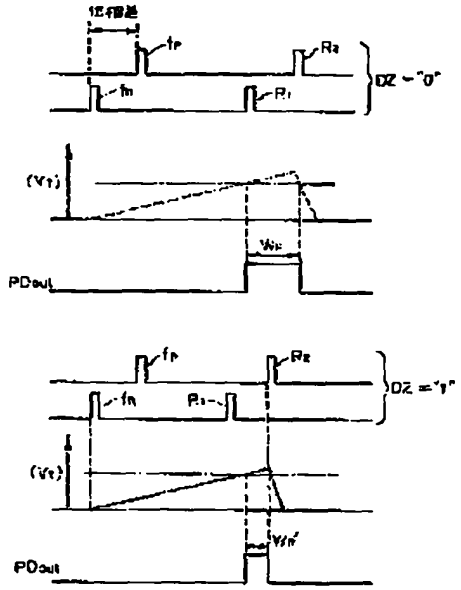
【図5】


fp
fR
DZ
DZ
25
29
23
28
24
22
26
27
Vpc
21
oPD

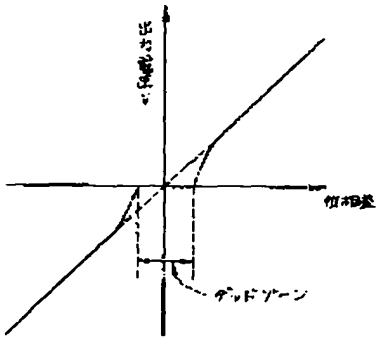
【図6】


(A)
(B)
(C)
(D)
(E)
fp
fR
R2
R1
DZ ="0"
To
①
②
(Vt)
PDout
R3
DZ ="1"

【図7】


位相差
fp
fR
R2
R1
DZ ="0"
(Vt)
PDout
R3
DZ ="1"

【図8】


位相差
デッドゾーン

【手続補正書】
【提出日】平成6年1月10日
【手続補正1】
【補正対象書類名】明細書
【補正対象項目名】発明の名称
【補正方法】変更
【補正内容】
【発明の名称】　PLL回路
【手続補正2】
【補正対象書類名】明細書
【補正対象項目名】特許請求の範囲
【補正方法】追加
【補正内容】
【特許請求の範囲】
【請求項1】　電圧制御発振手段と、この発振出力周波数信号と外部発振周波数信号との位相比較をなす位相比較手段と、この位相比較出力に応じて前記電圧制御発振手段の制御電圧を生成する制御電圧生成手段とを含むPLL回路であって、前記制御電圧生成手段は、前記位相比較出力を遅延する遅延手段と、前記位相比較出力を入力とする時定数回路と、前記遅延手段の出力によって前記時定数回路の出力状態をラッチし前記遅延手段の出力が消失したときにこのラッチ状態を解除するラッチ手段とを含み、このラッチ出力を用いて前記制御電圧を生成するよう構成されていることを特徴とするPLL回路。
【請求項2】　前記位相比較手段は、前記発振出力周波数信号と外部発振周波数信号との一方に対する他方の位相ずれを検出して位相進み及び移相遅れに夫々対応した位相比較出力を生成するよう構成されており、前記遅延手段、前記時定数回路及びラッチ手段の各々は前記位相進み及び位相遅れに対応した位相比較出力に夫々対応して設けられていることを特徴とする請求項1記載のPLL回路。
【請求項3】　前記遅延手段の遅延時間は、前記位相比較における不感帯（デットゾーン）に相当する時間に設定されていることを特徴とする請求項1または2記載のPLL回路。
【手続補正3】
【補正対象書類名】明細書
【補正対象項目名】0006
【補正方法】変更
【補正内容】
【0006】次に動作について説明する。D－FF22の入力端子D1には、D－FF23反転出力Q2が印加され、D－FF23の入力端子D2にはD－FF22の反転出力Q1が印加され、出力Q1はチャージポンプ回路21のNMOS26のゲートに印加され、出力Q2はNMOS27のゲートに印加される。
【手続補正4】
【補正対象書類名】明細書
【補正対象項目名】0015
【補正方法】変更
【補正内容】
【0015】デッドゾーンを設けることにより、PLL回路がロックしている状態でVCOの外乱となるような制御パルスの頻繁な発生が防止され、またジッタノイズ等の雑音信号もカットされ、S／Nを大幅に改善している。
【手続補正5】
【補正対象書類名】明細書
【補正対象項目名】0017
【補正方法】変更
【補正内容】
【0017】例えば、fRがfPに対して12nsec早くなった場合を想定すると、図7に示す様になる。Dz＝"0"のデッドゾーン0の状態では、出力Q1がVτを越えている時間は約12nsecとみることができ、Pd信号として"1"が12nsec出力されるが、Dz＝"1"のデッドゾーン10nsecの状態では、出力Q1がVτを越える時間は約2nsecとなり、Pd信号として「1」は2nsec間しか続かず、ループフィルタを通してのVCOの制御を行う積分電圧値の変化の割合が遅くなる。